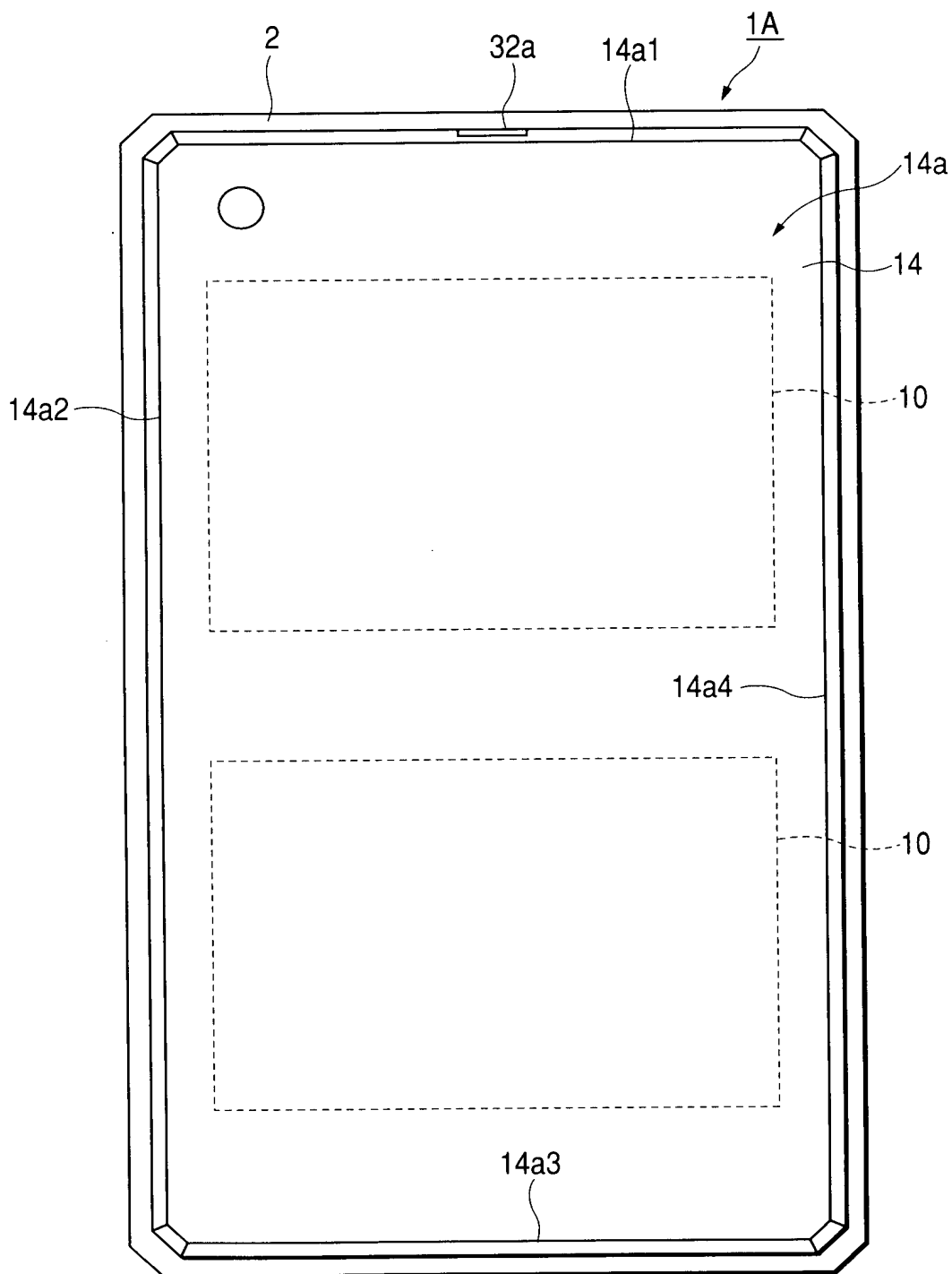
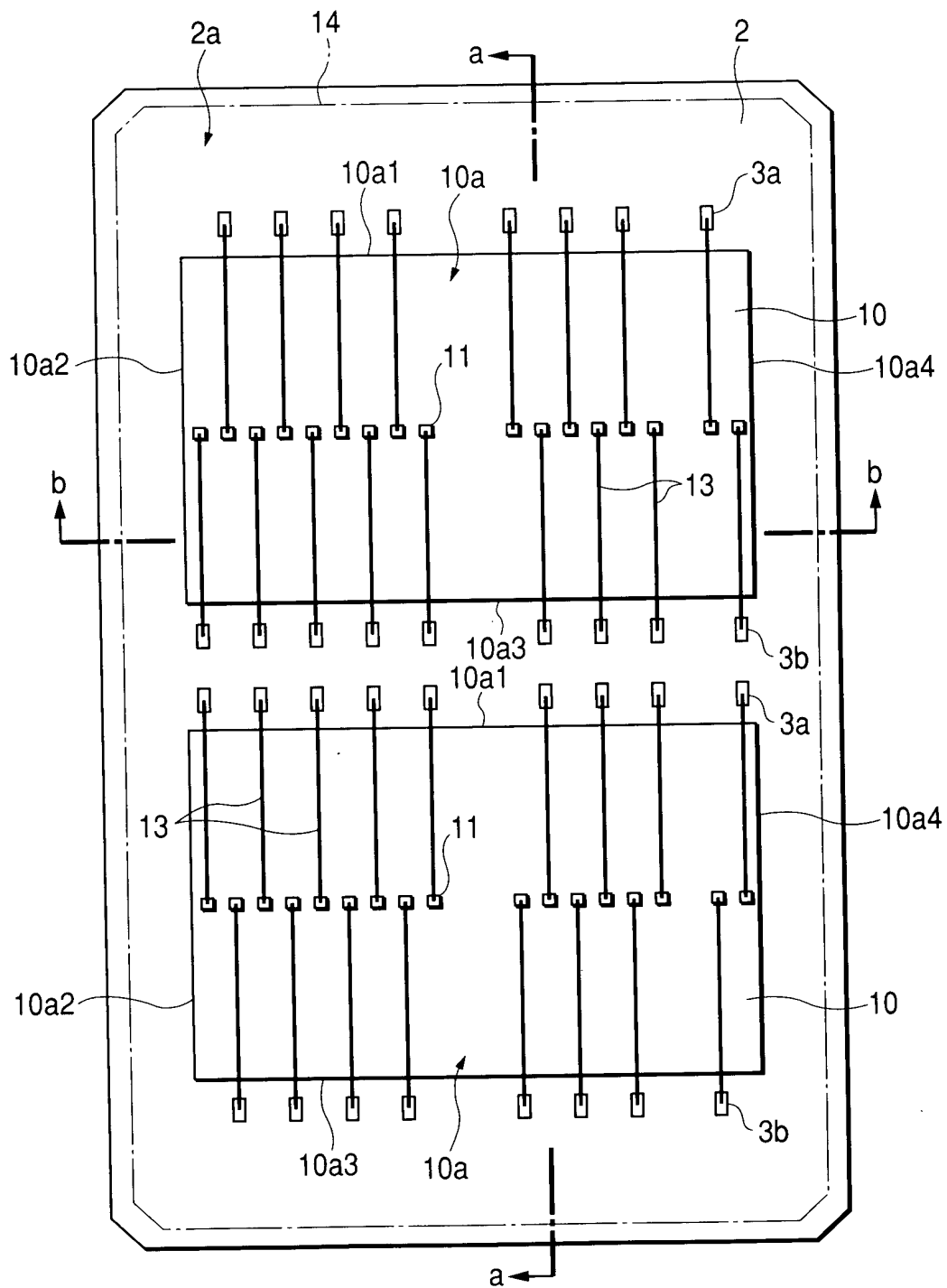


**FIG. 1**



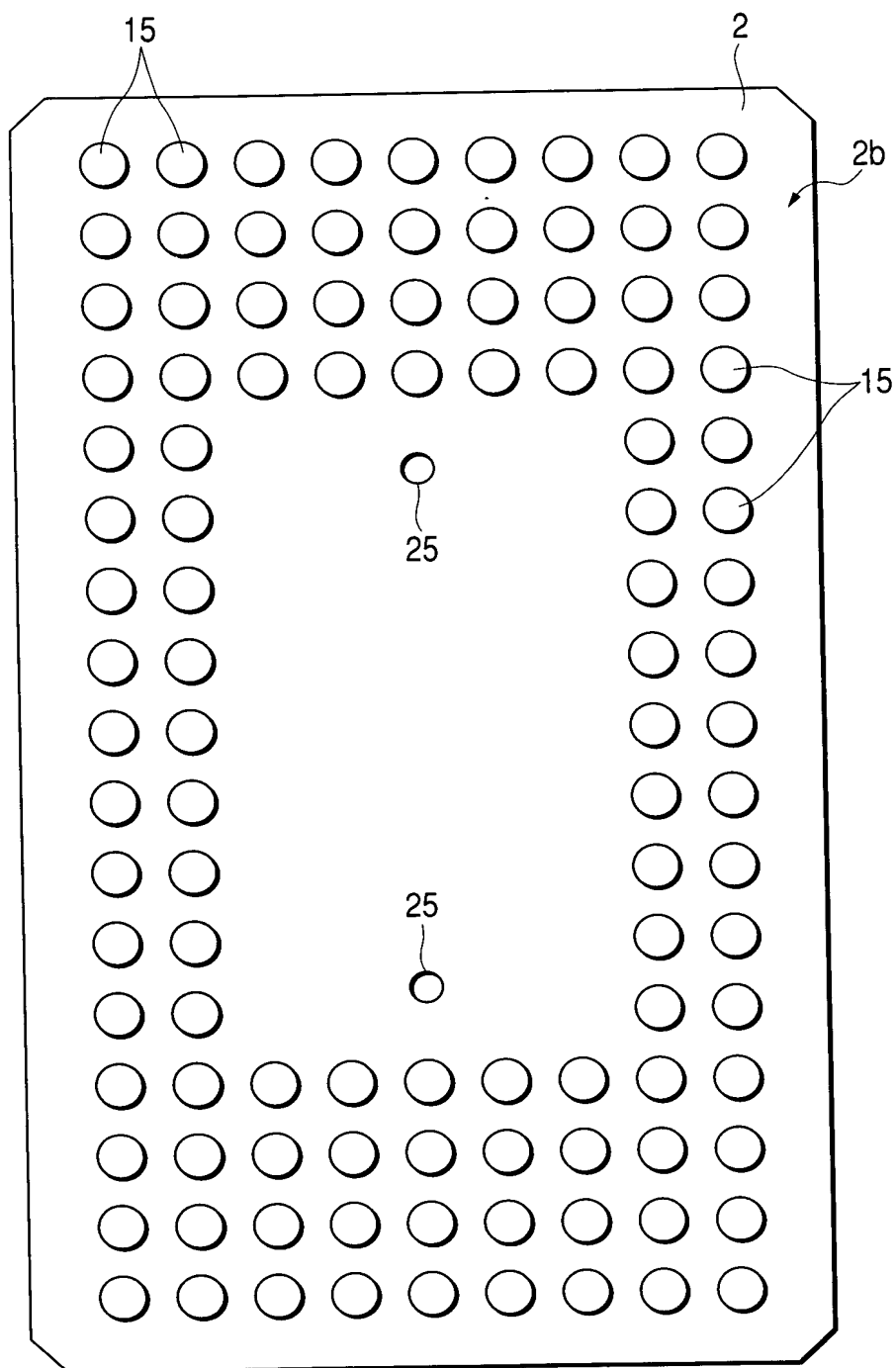
20200924T600T

FIG. 2



2020091426-030702

**FIG. 3**



10091426.030702

The diagram illustrates a semiconductor device in cross-section. It features a central channel region 10 flanked by two side regions, 10a on the left and 10a1 on the right. These regions are separated by a vertical barrier or gate structure 10a3. Above the channel, there is a gate stack 14, which includes a gate dielectric 14a and a gate electrode 14a1. Below the channel, there is a substrate 8. Source and drain regions 11 are located on either side of the channel. Contact pads 15 are provided for electrical connection to the source and drain regions. Other labels include 2, 3a, 3b, 10a, 10a1, 10a3, 14a, and 14a1, indicating different layers and components of the device.

FIG. 6

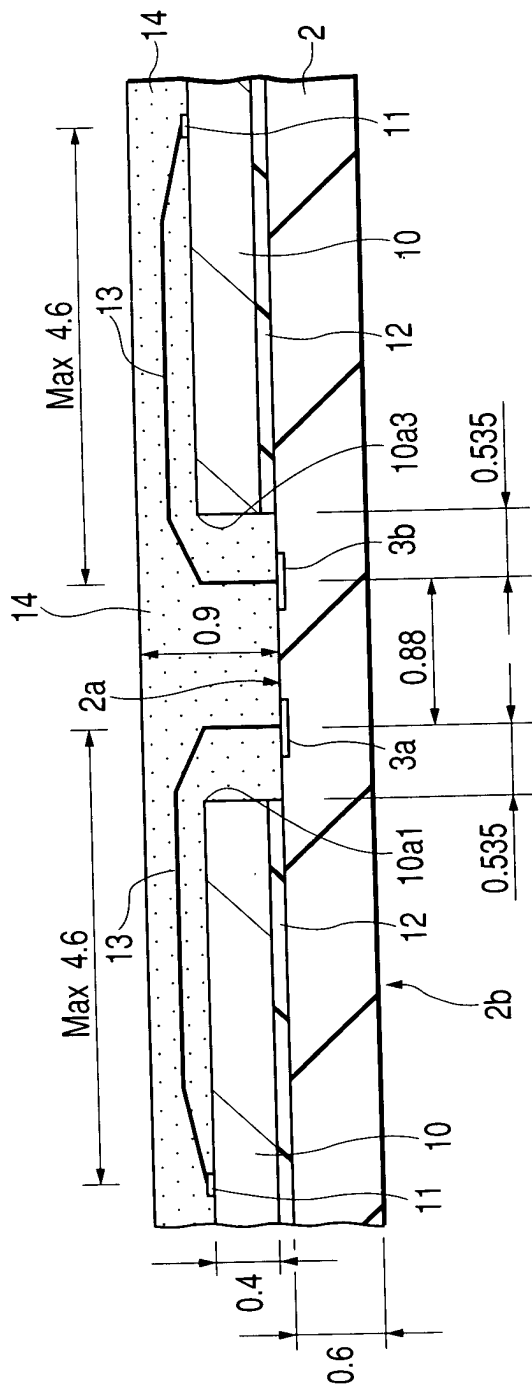
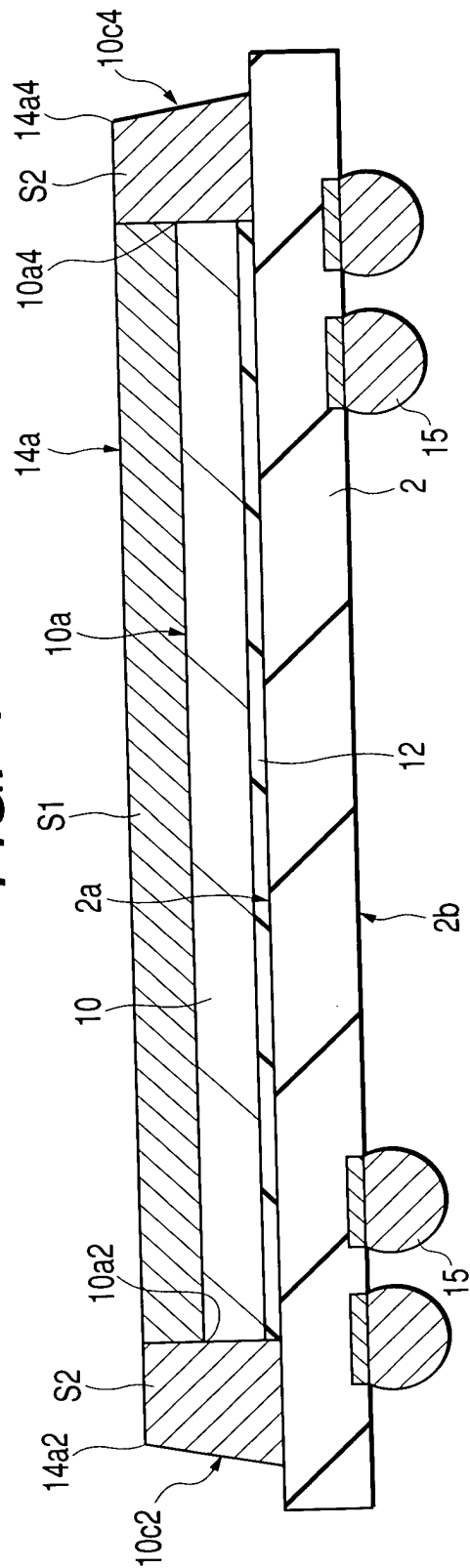


FIG. 7



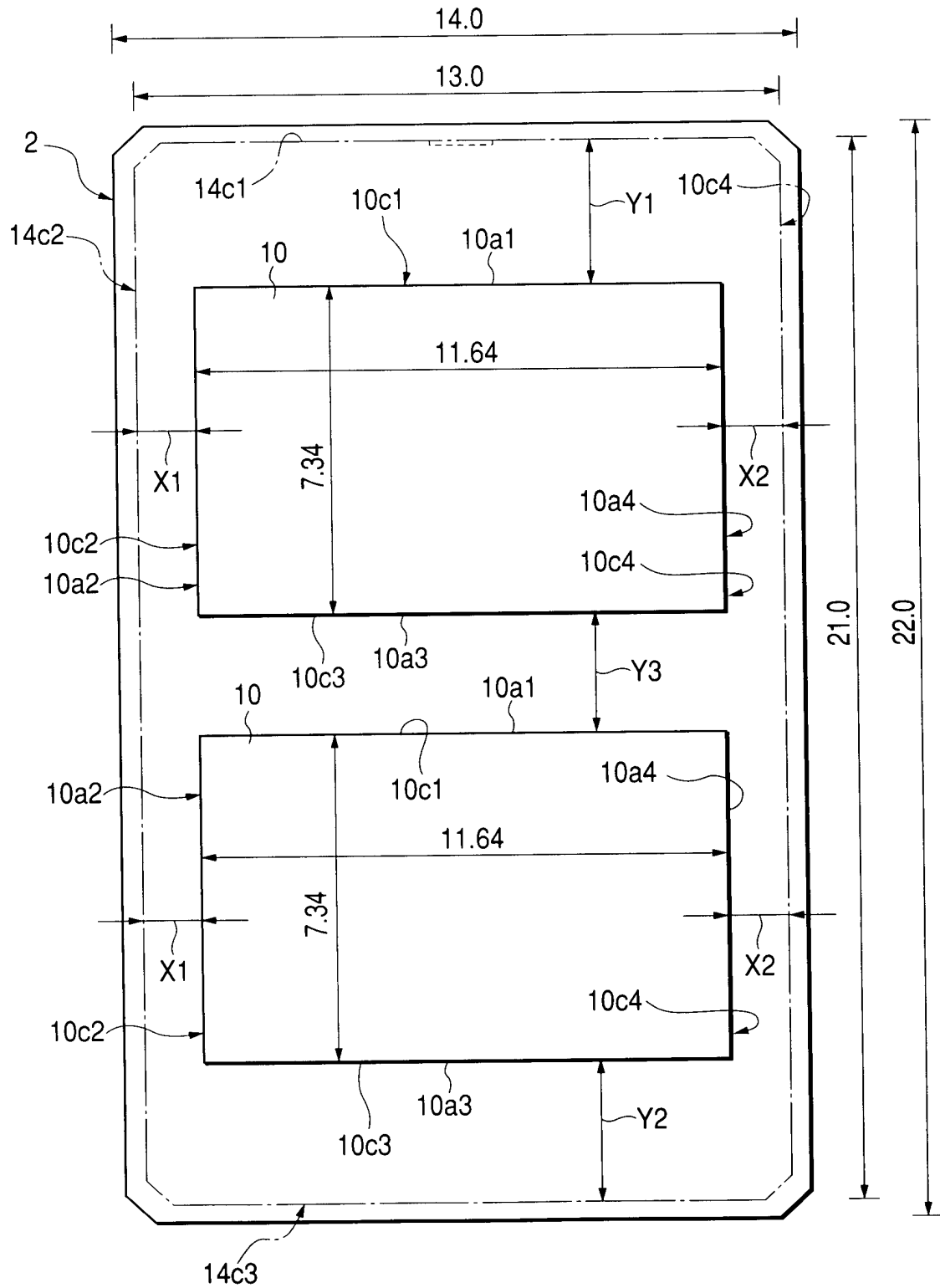
**FIG. 8**

FIG. 9

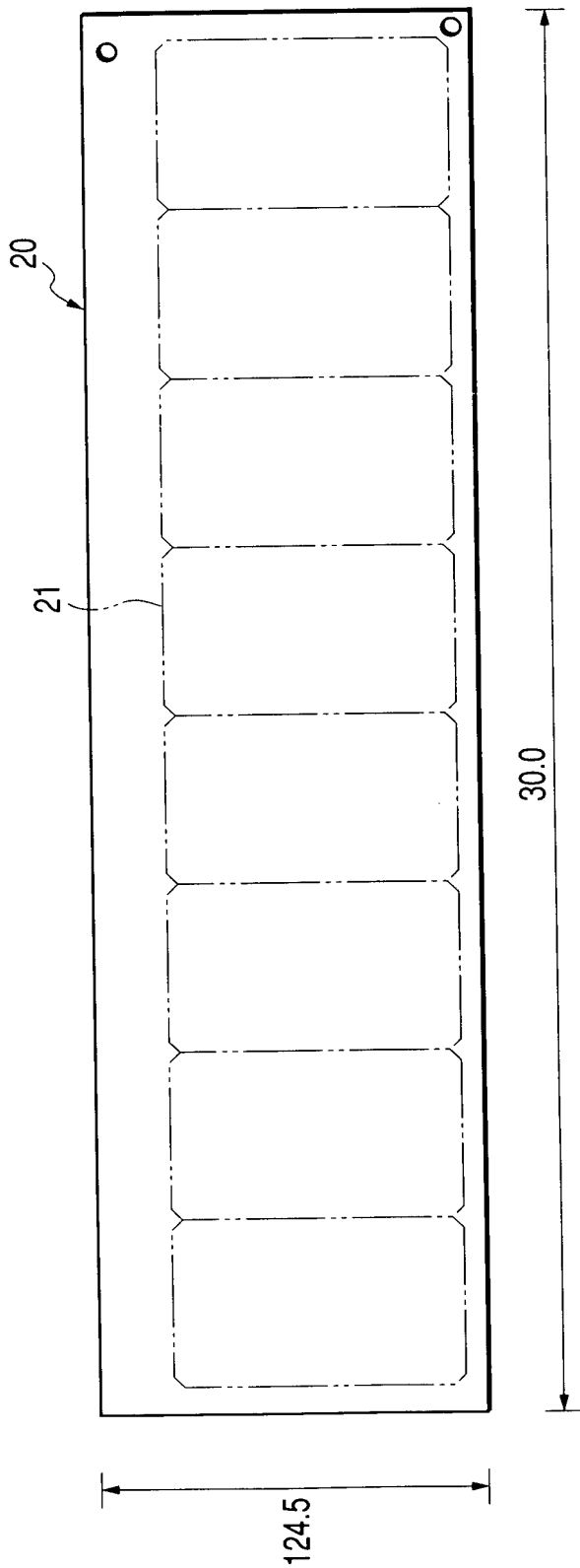


FIG. 10

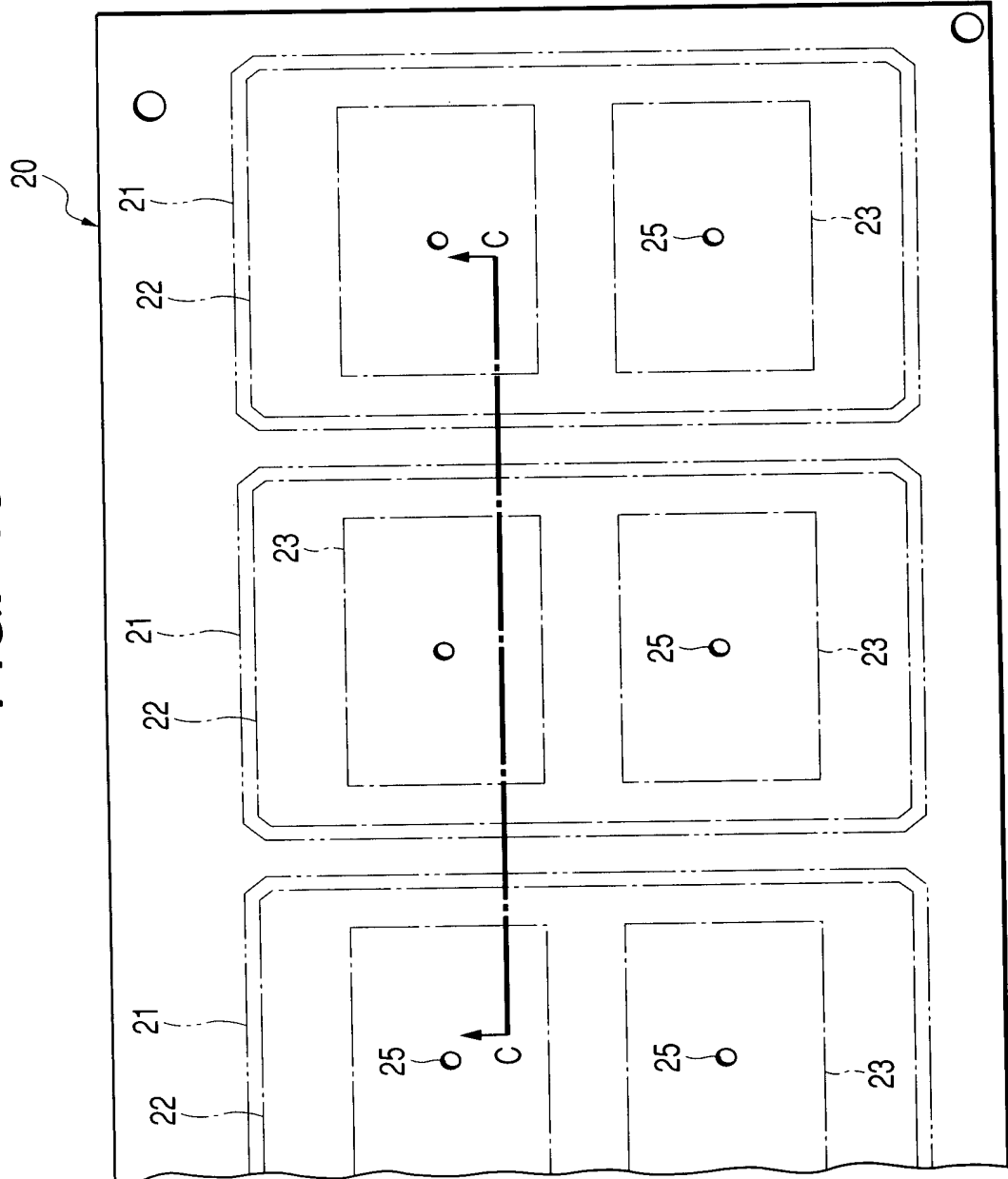




FIG. 11

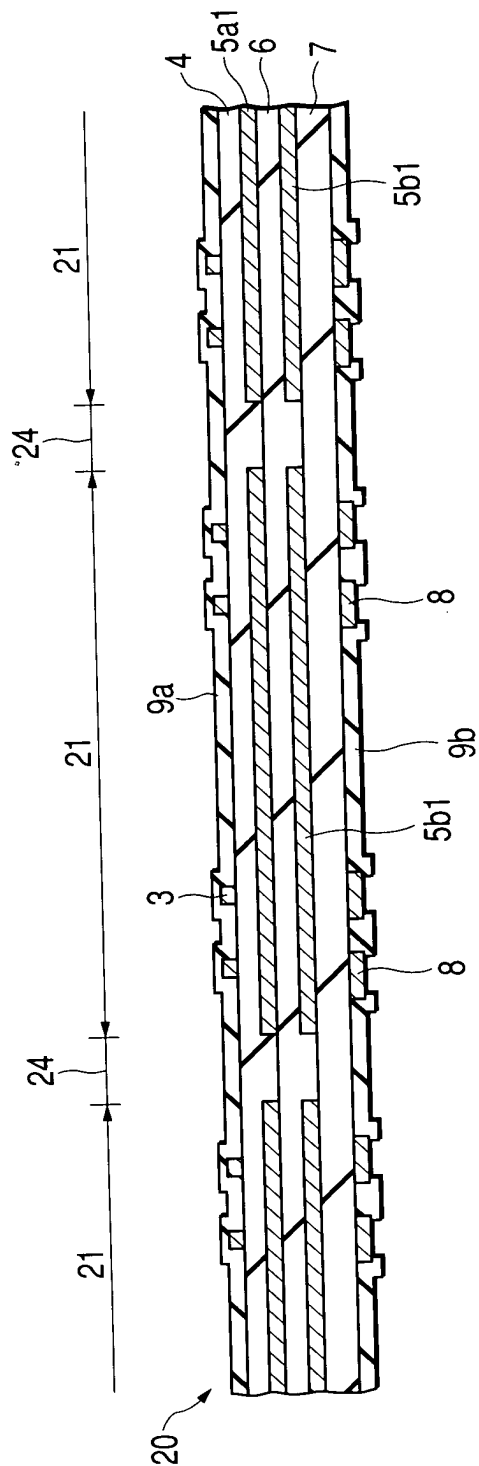


FIG. 12

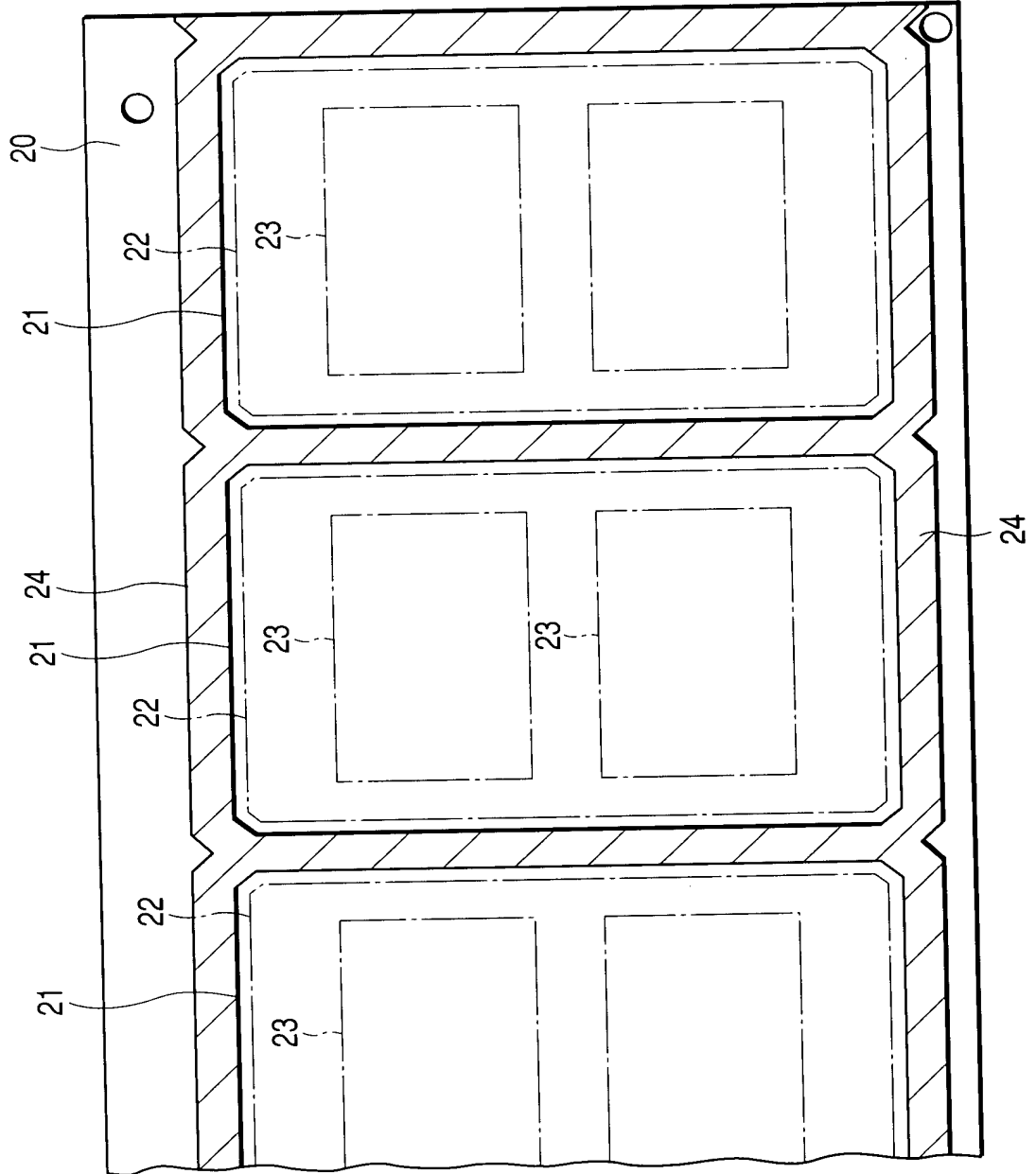


FIG. 13

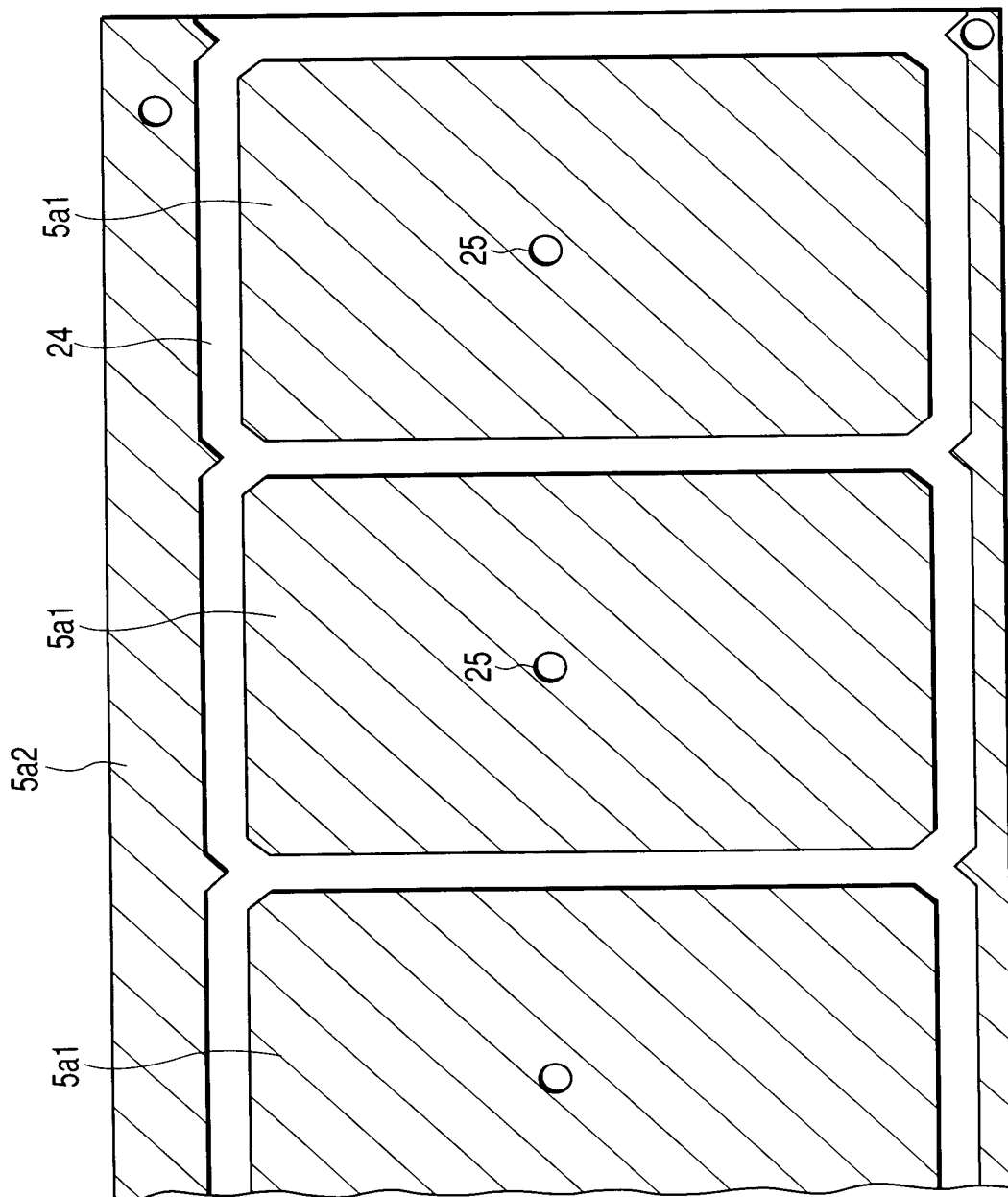


FIG. 14

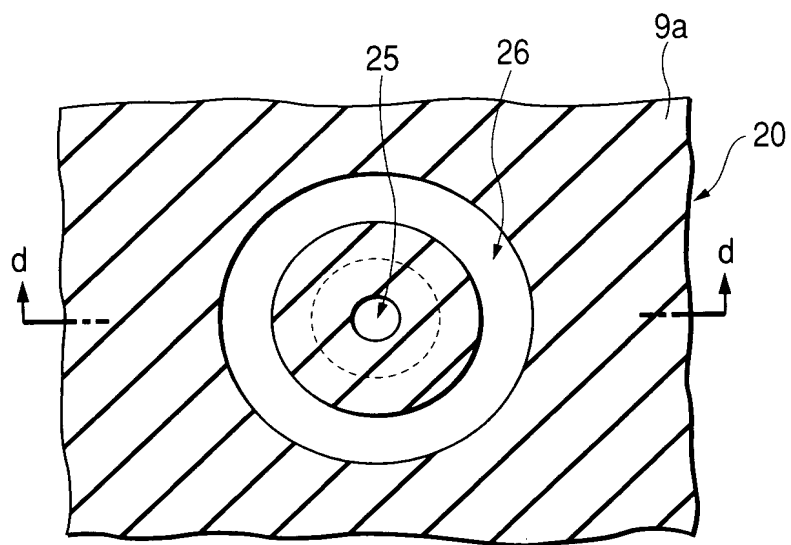


FIG. 15

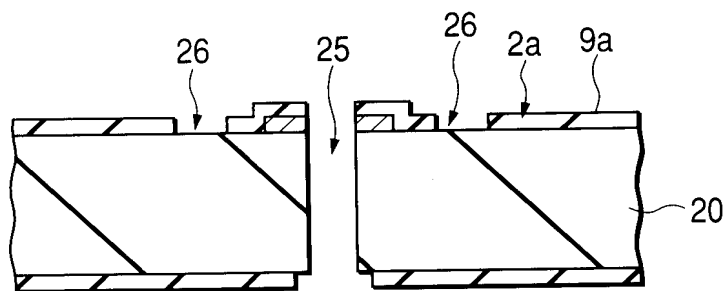


FIG. 16

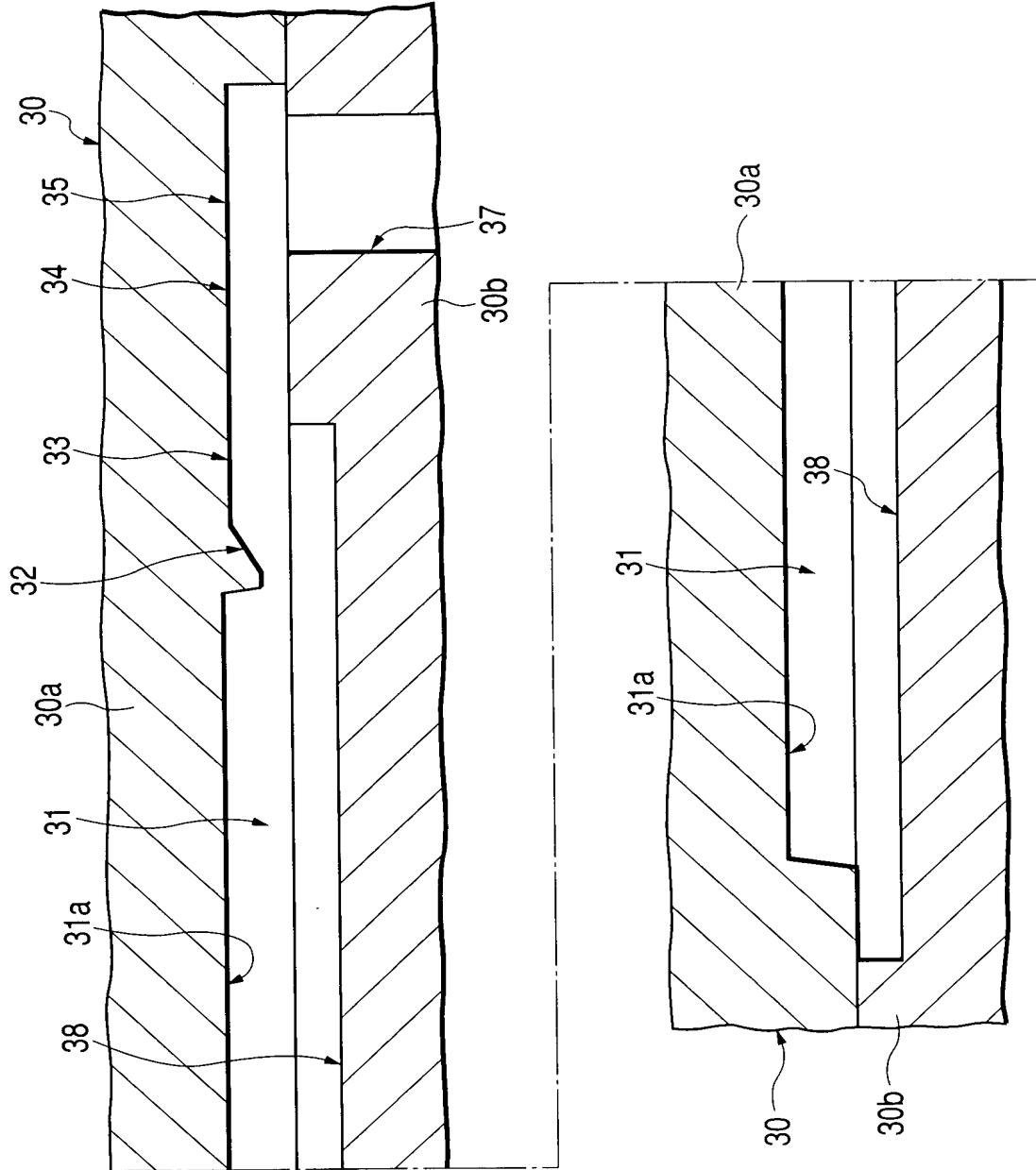


FIG. 17

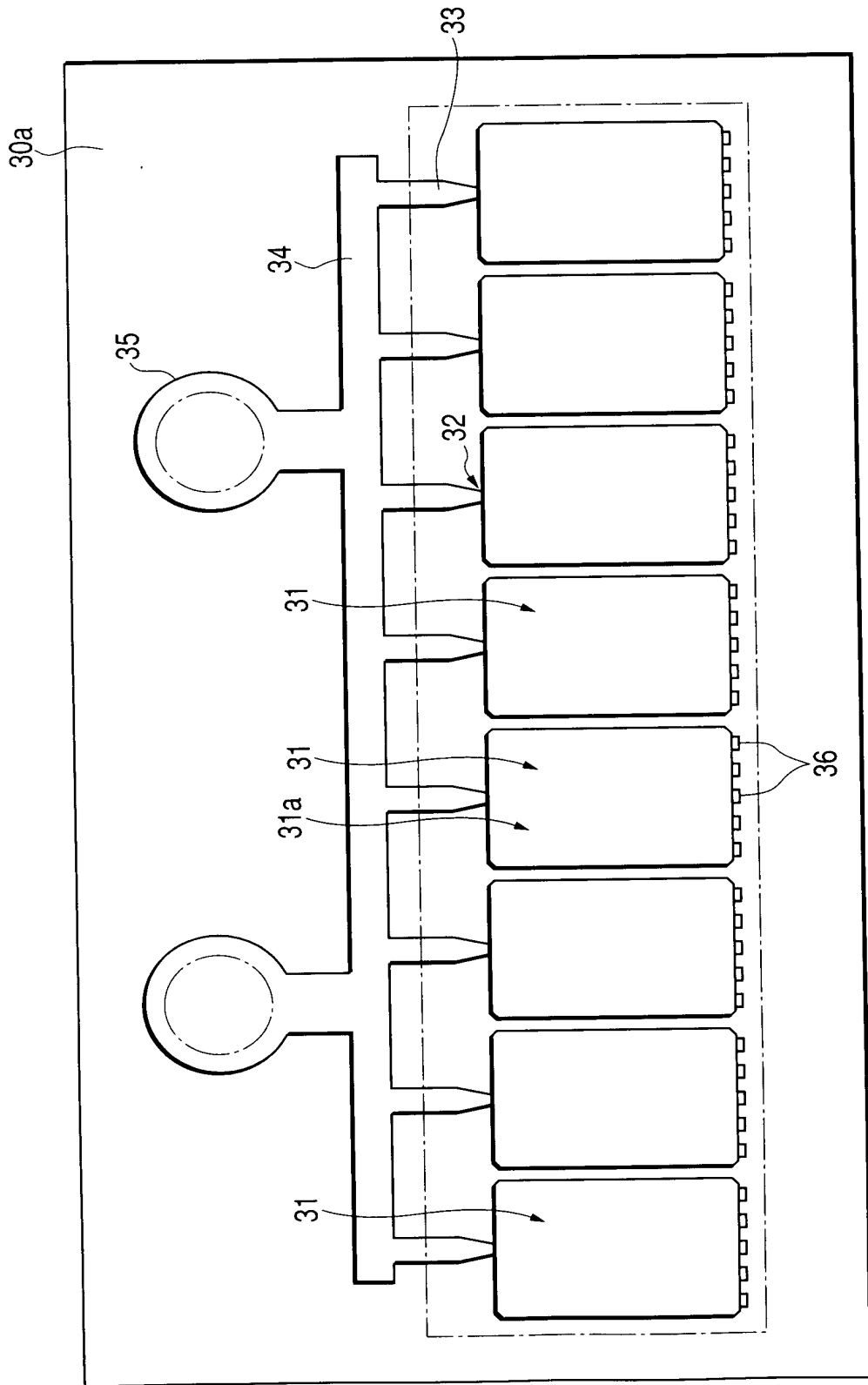


FIG. 18

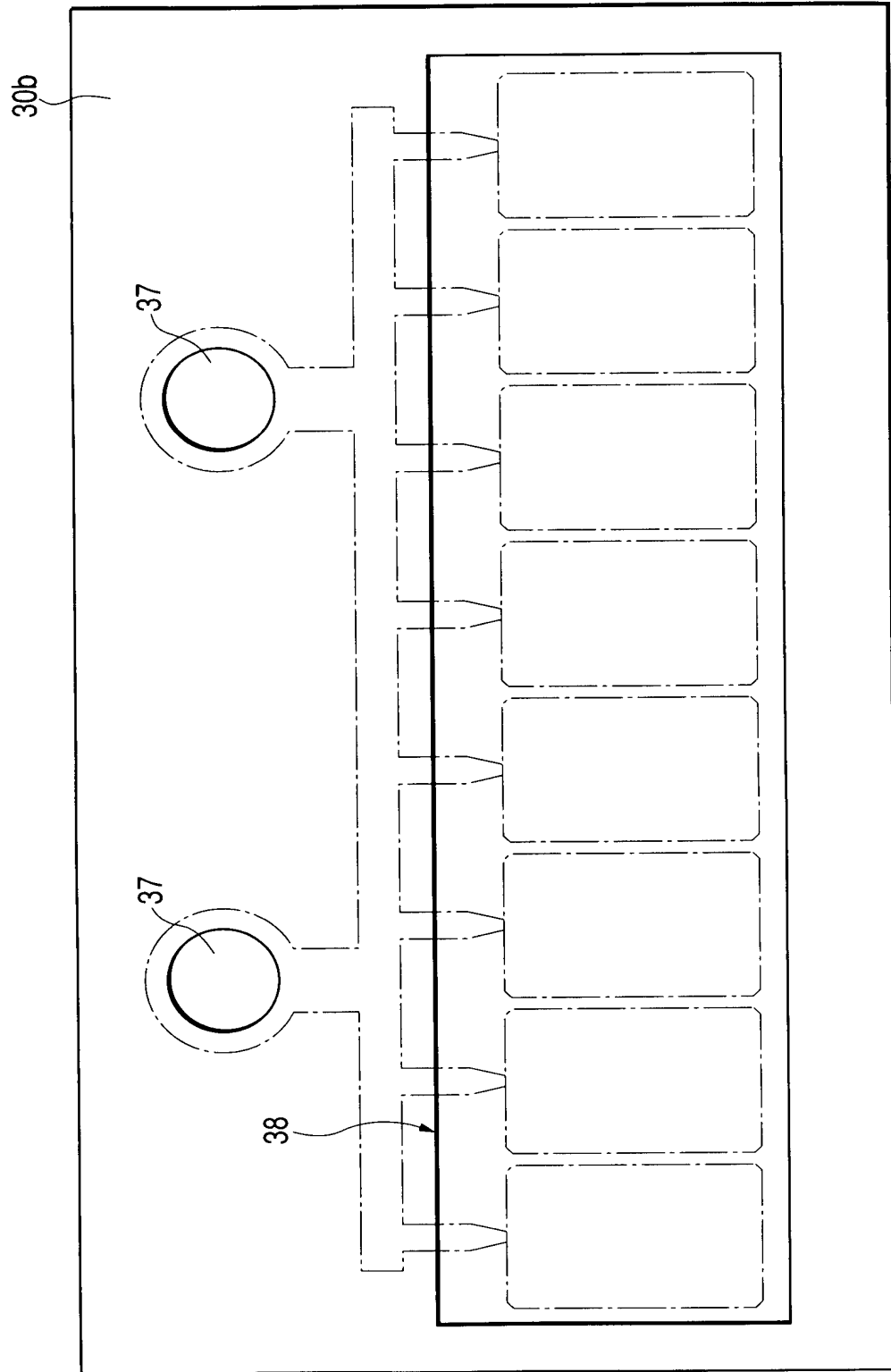
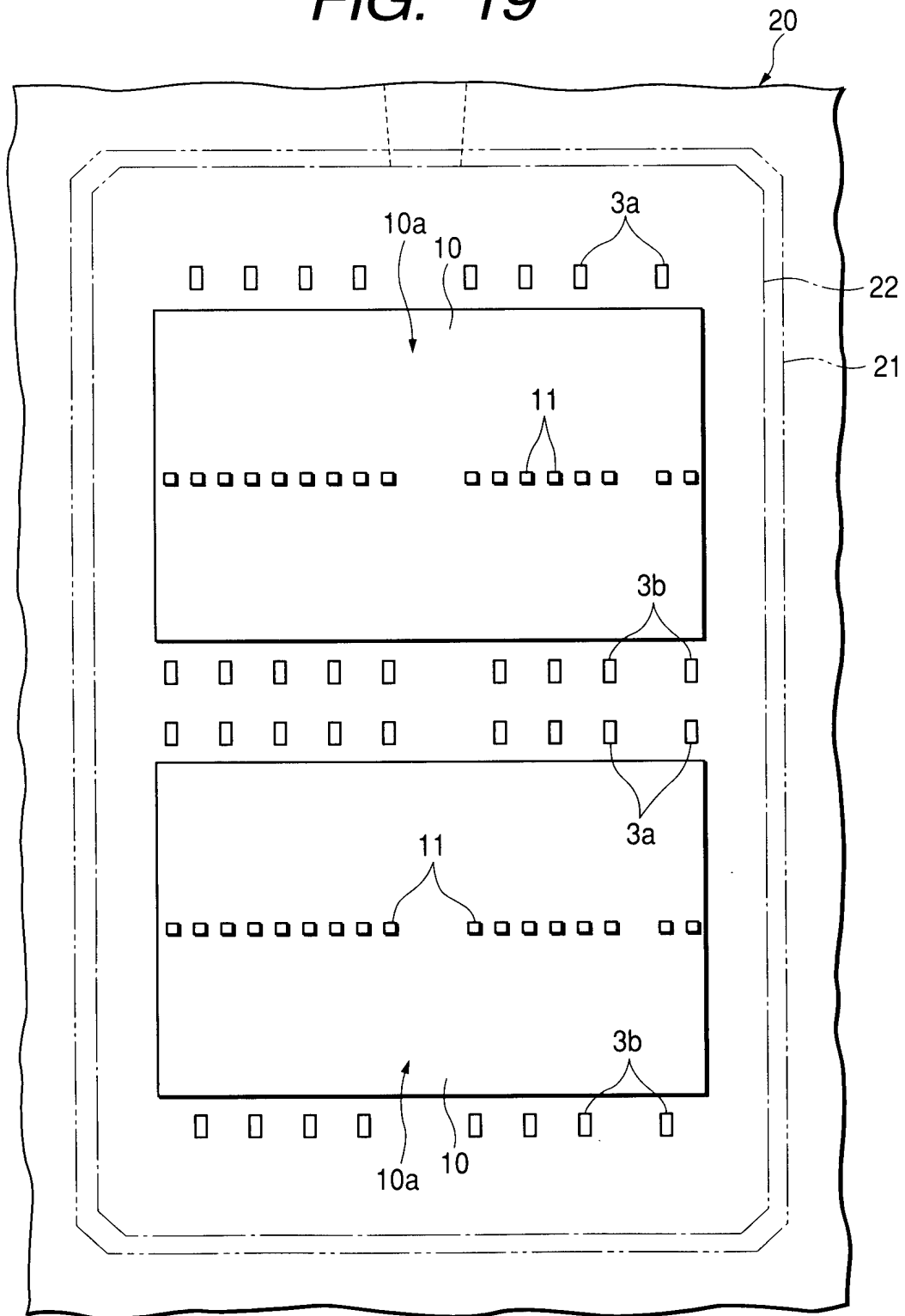


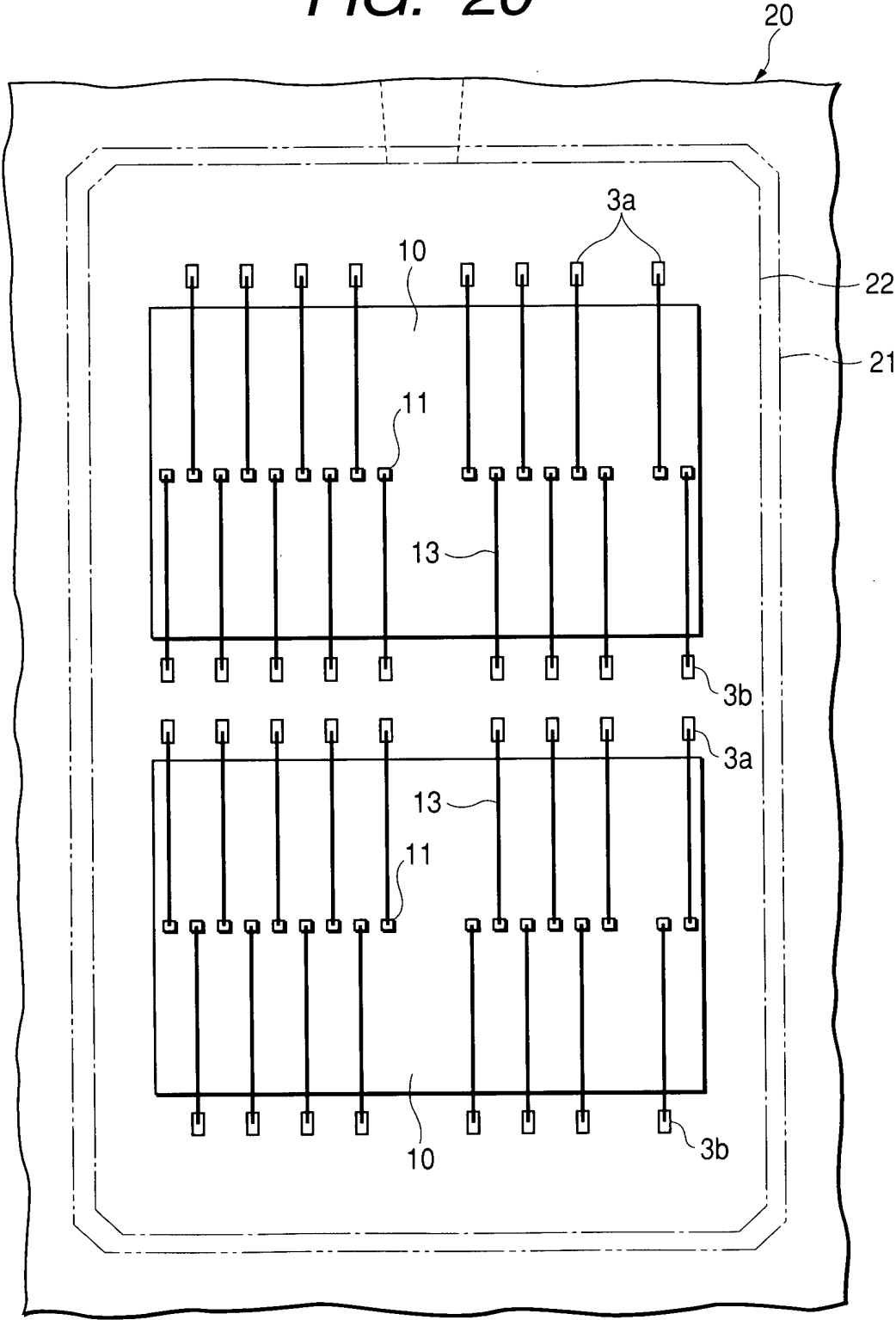
FIG. 19



10091426.030702



FIG. 20



10091426.030702

FIG. 21

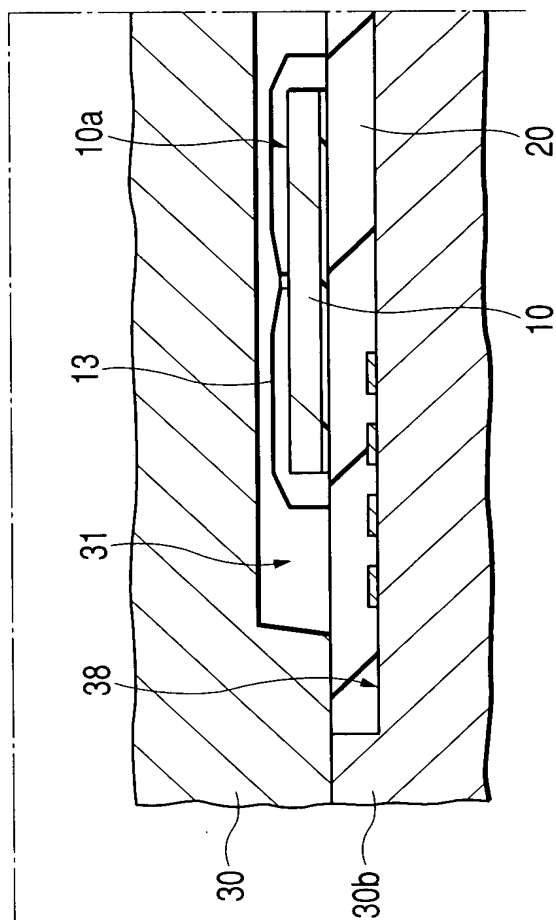
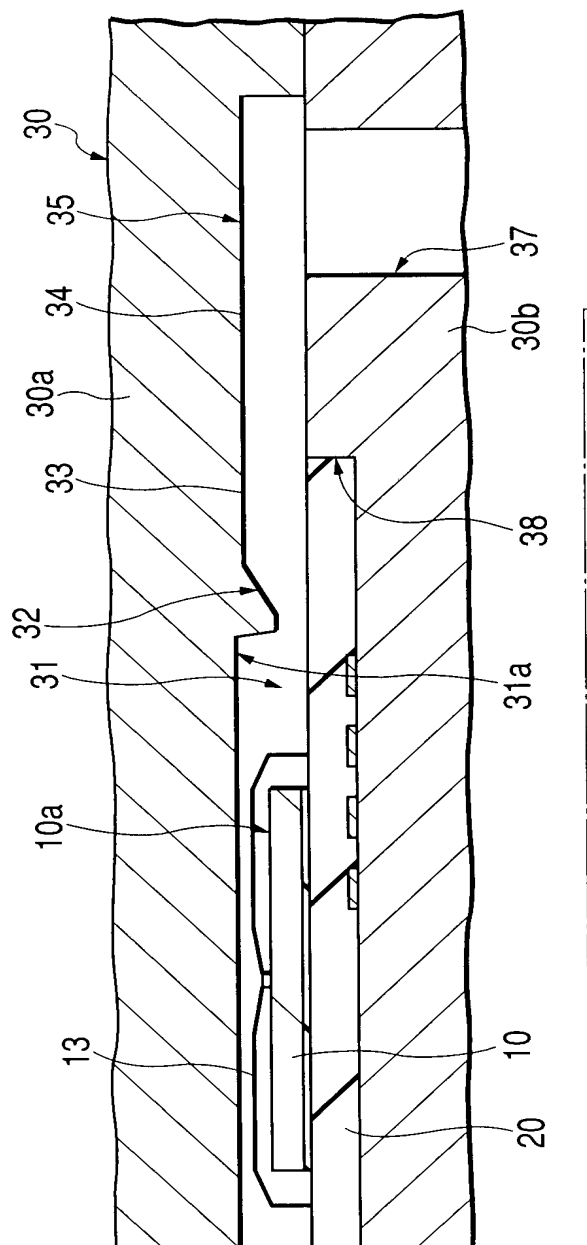
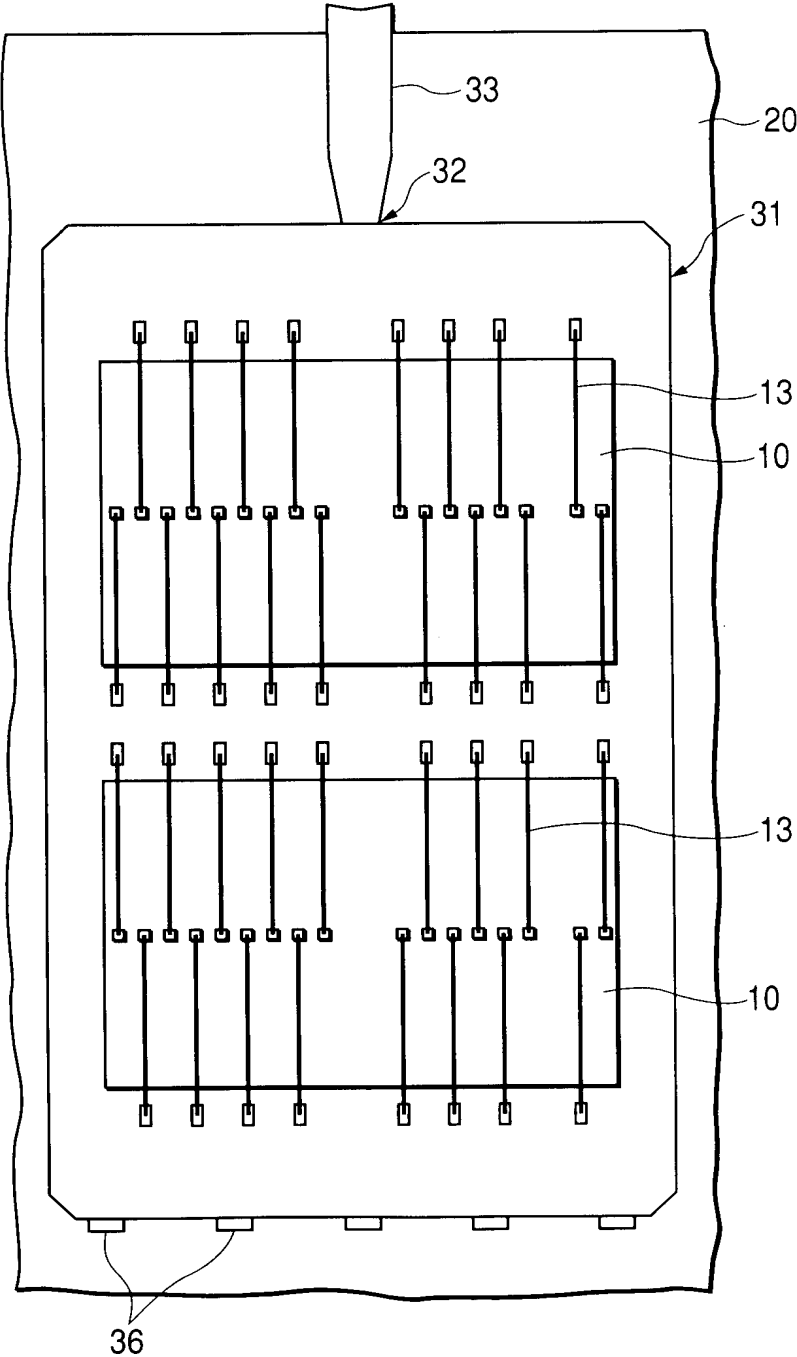
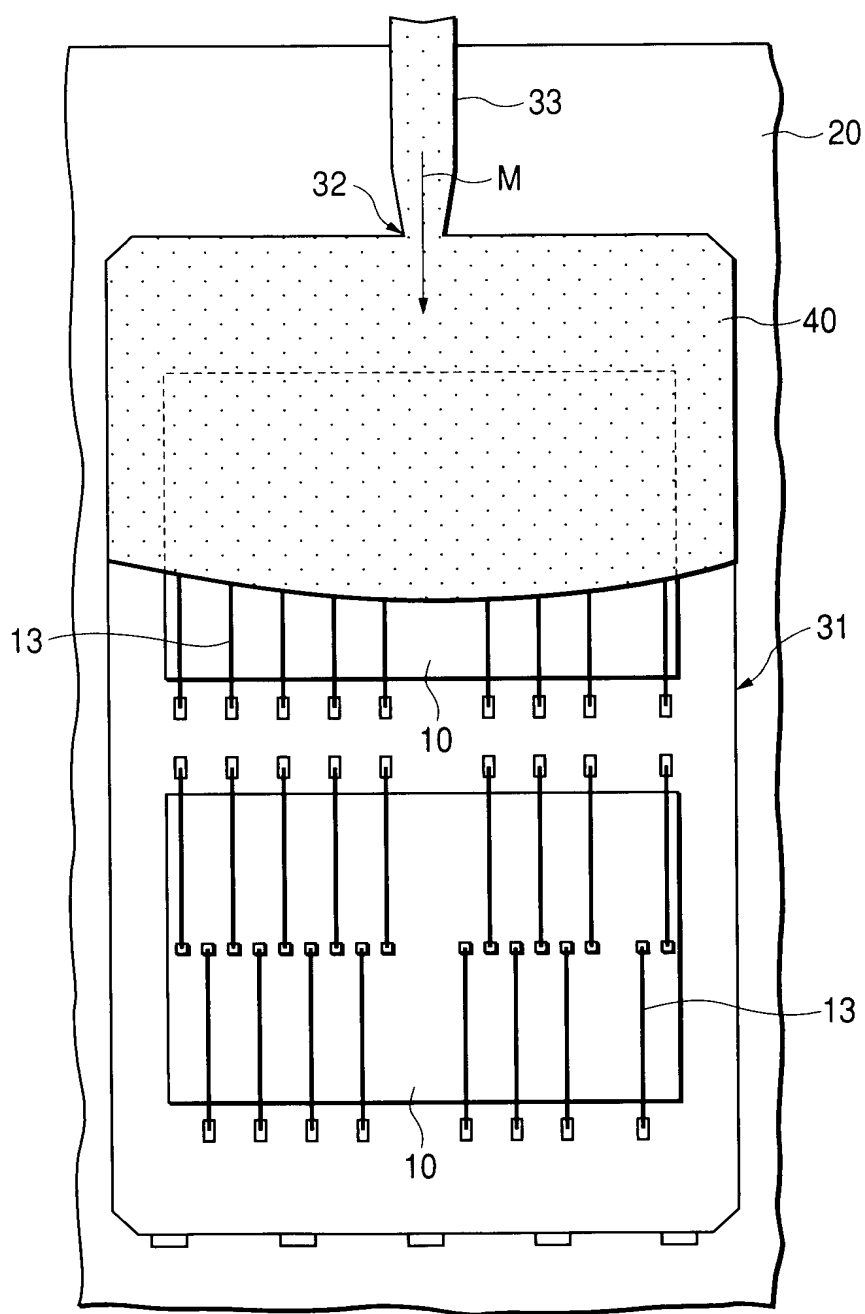


FIG. 22



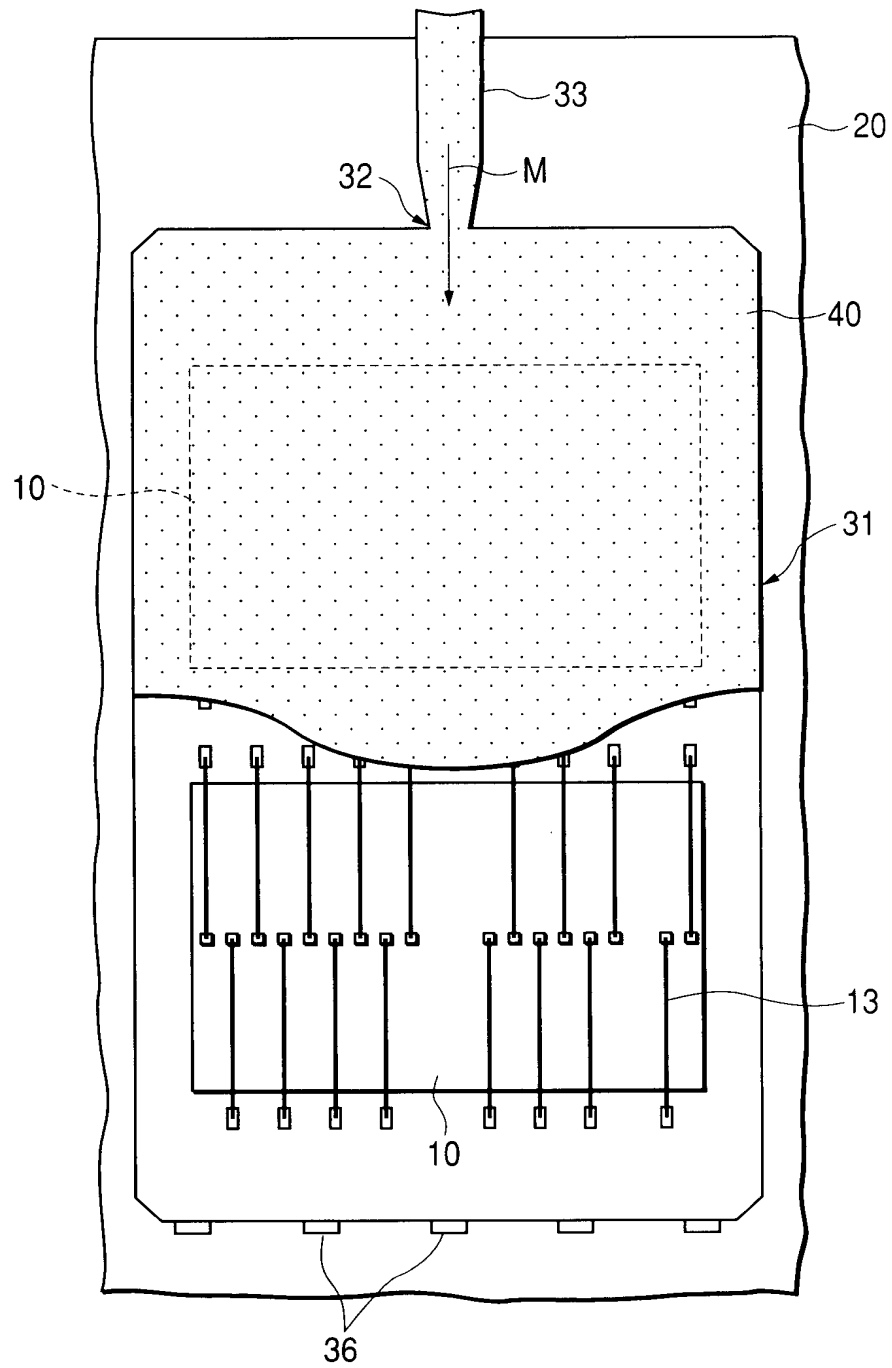
10094426.030702

FIG. 23



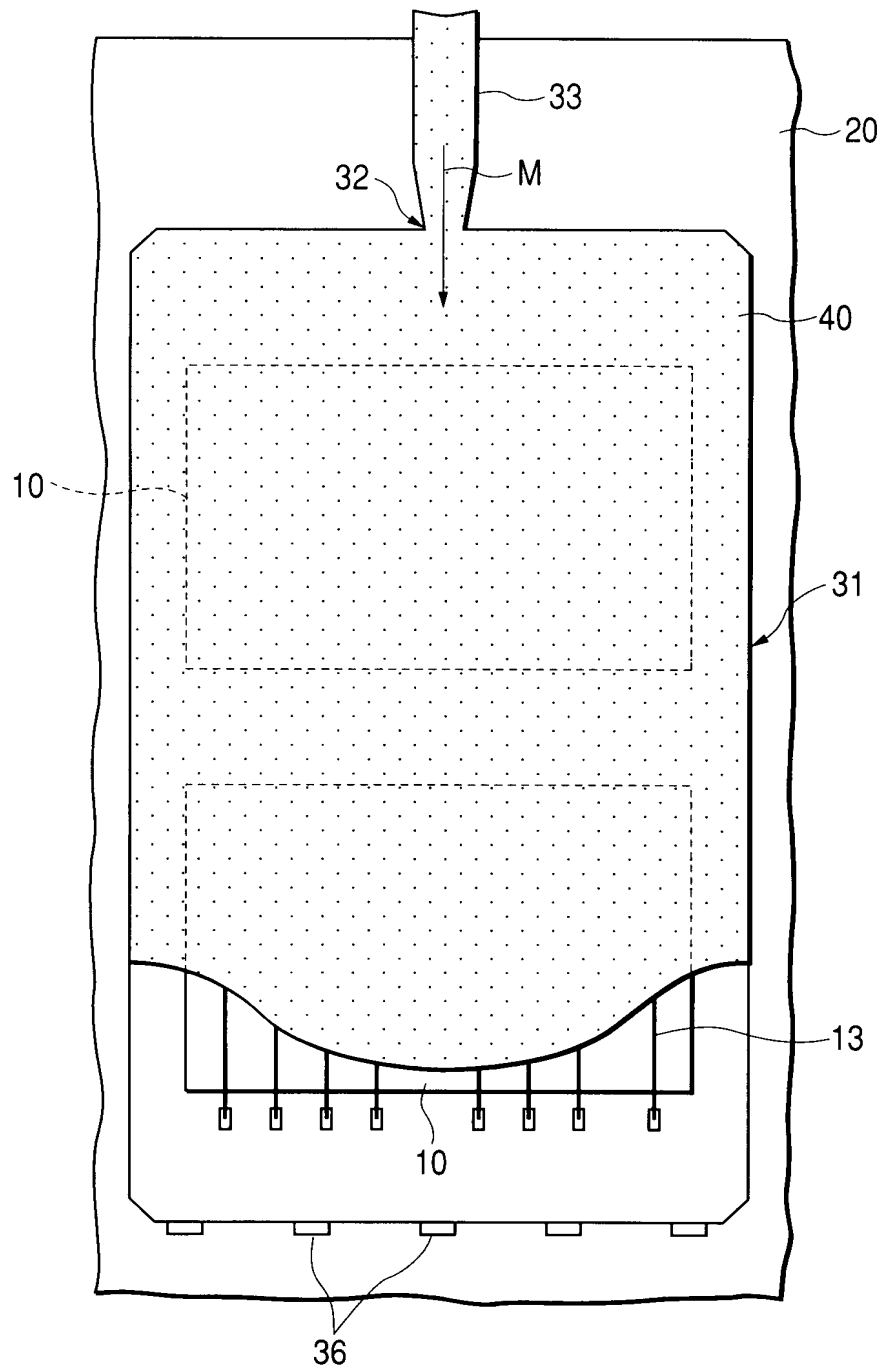
2020091426.030702

FIG. 24



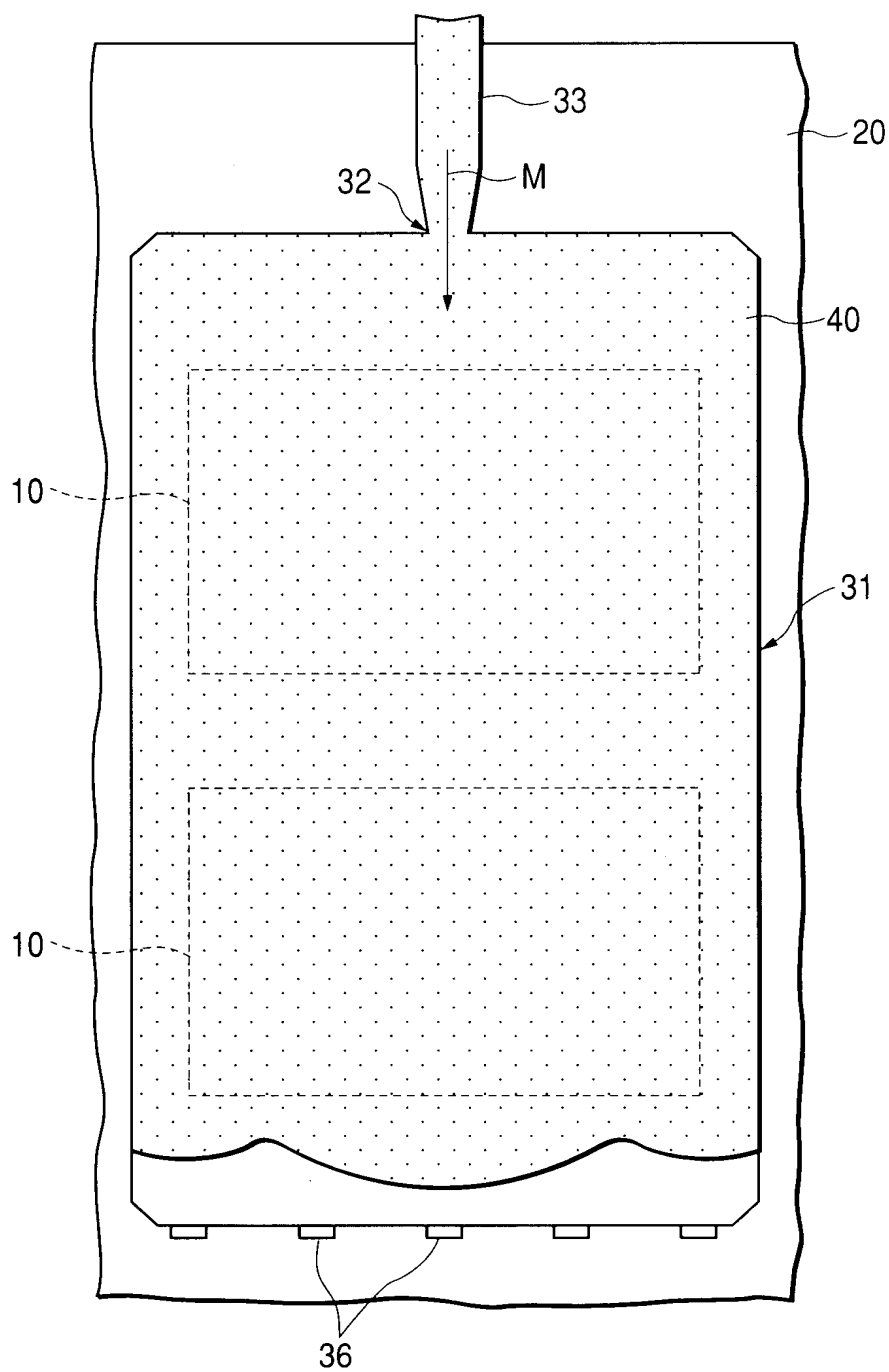
10091426.030702

FIG. 25



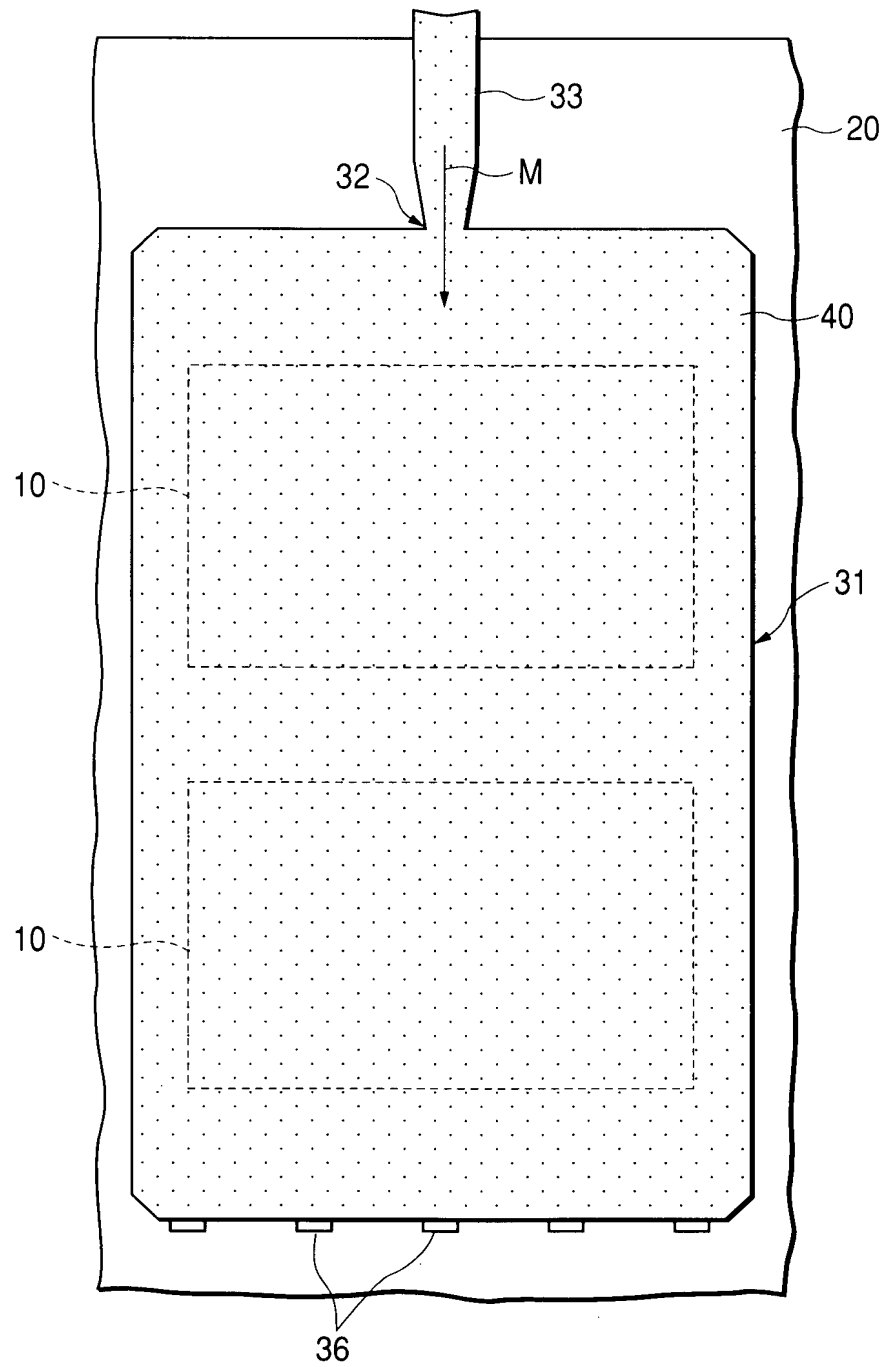
10091426.030702

**FIG. 26**



10091426, 030702

FIG. 27



10094426.030702



FIG. 28

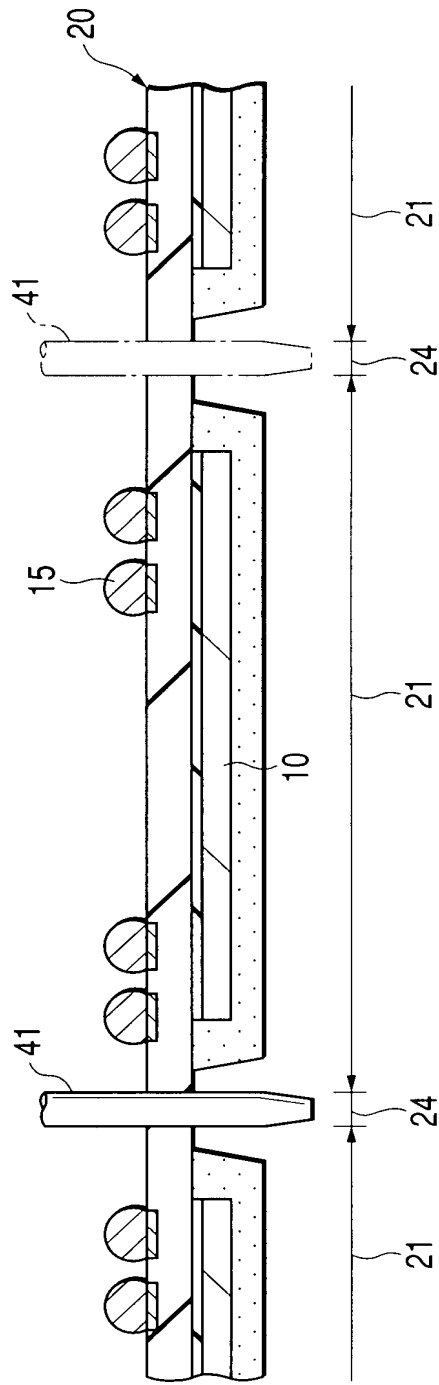
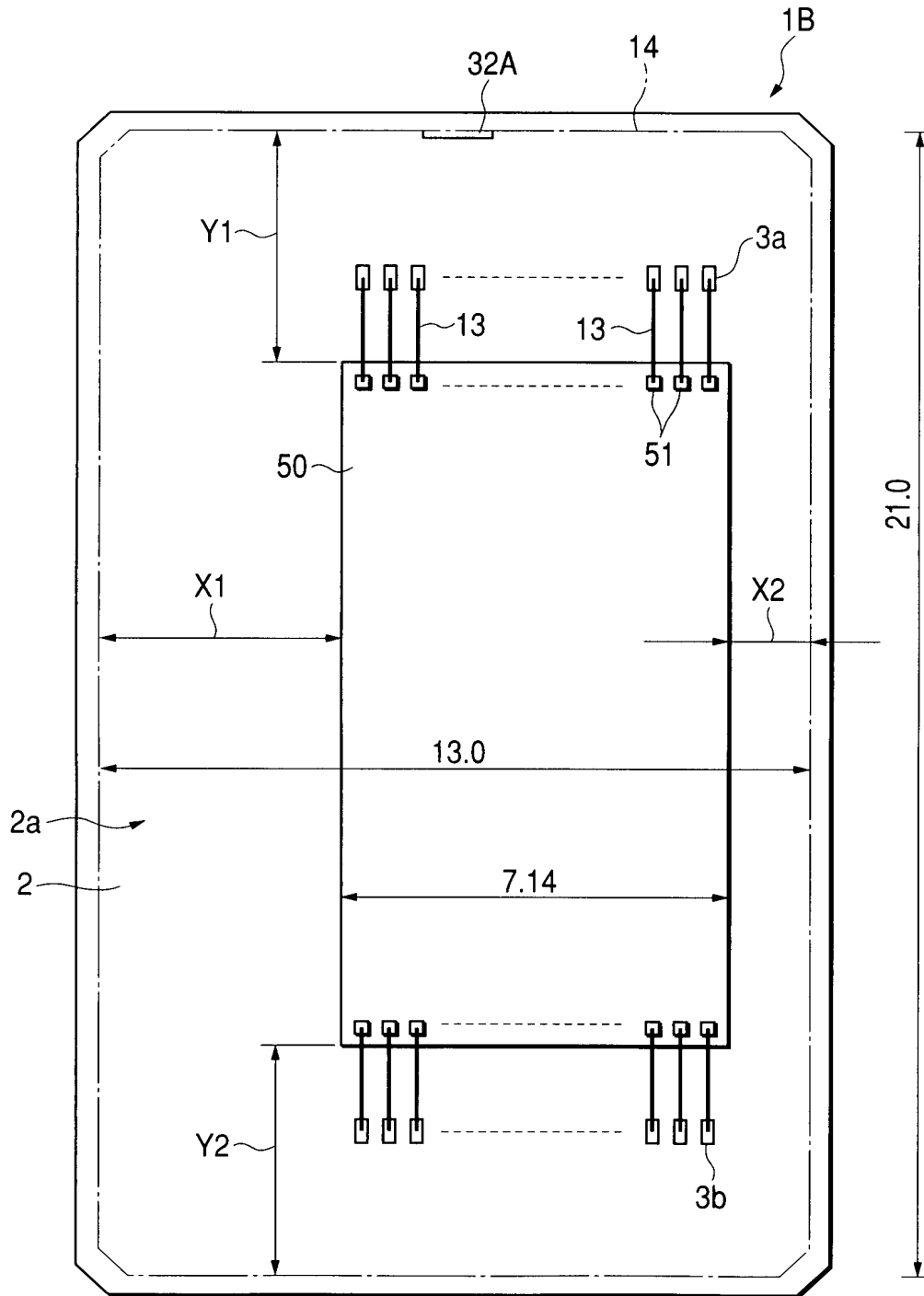
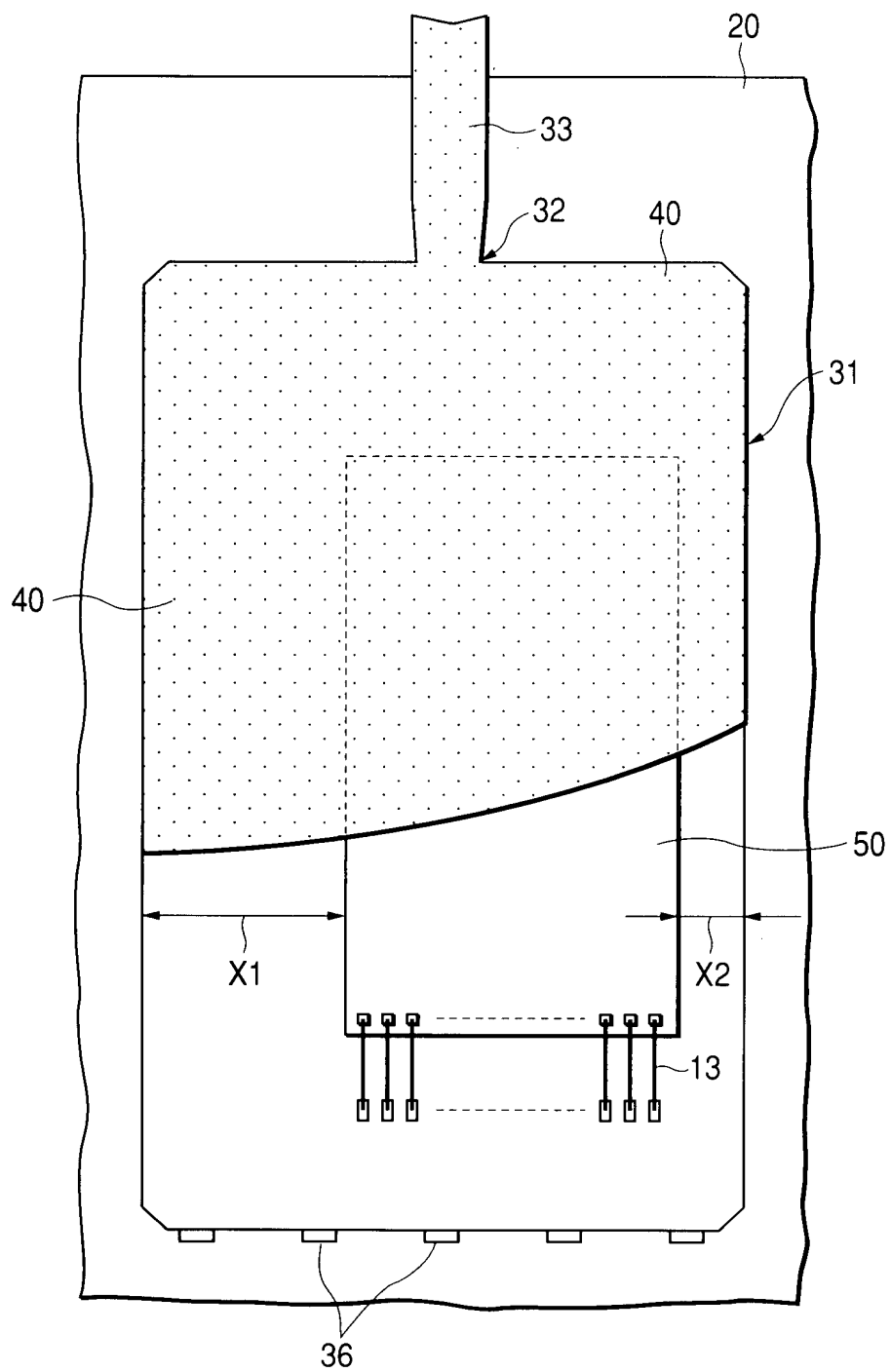


FIG. 29



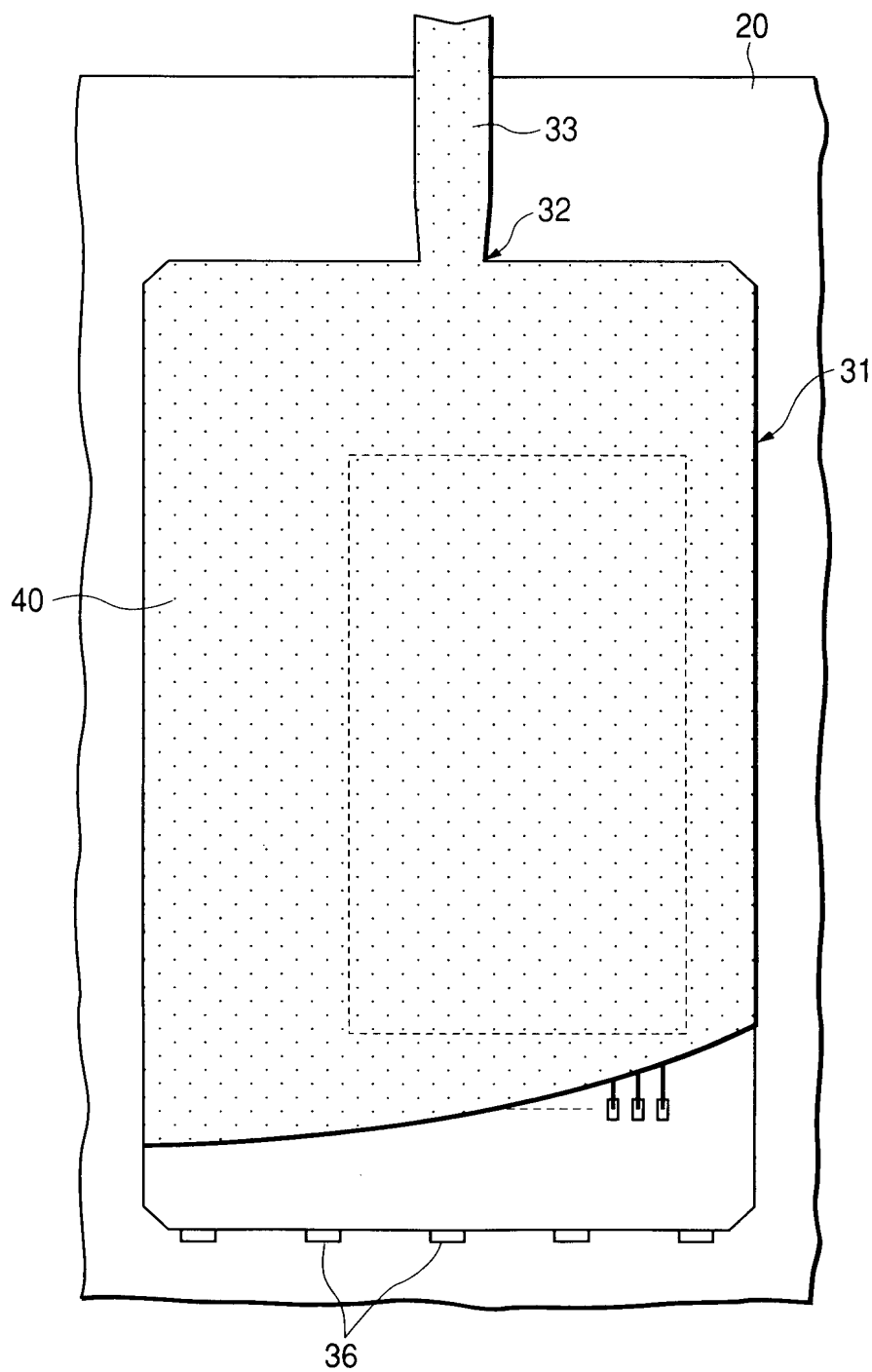
10091426.030702

FIG. 30



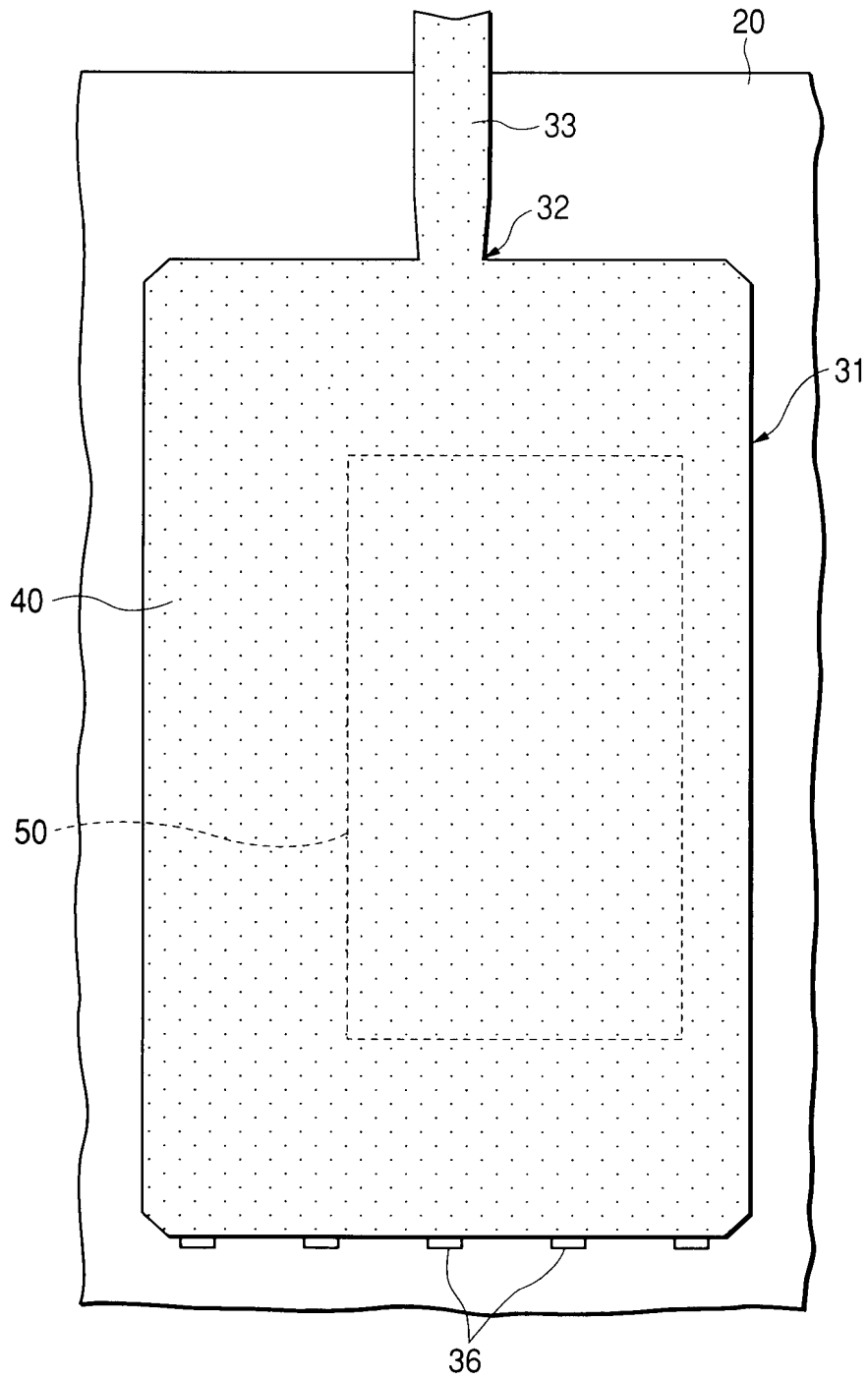
2020092416001

FIG. 31



20200909.030702

**FIG. 32**



10091426 "030702"

FIG. 33

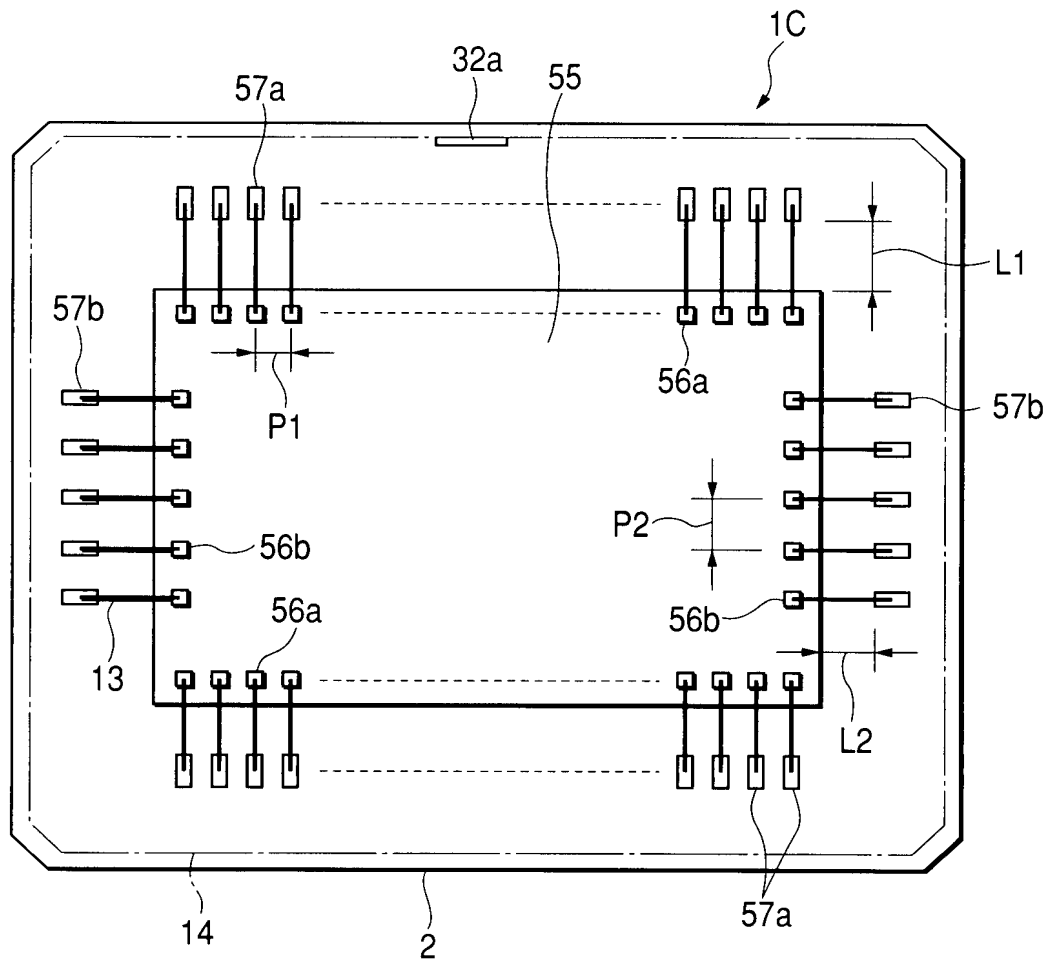
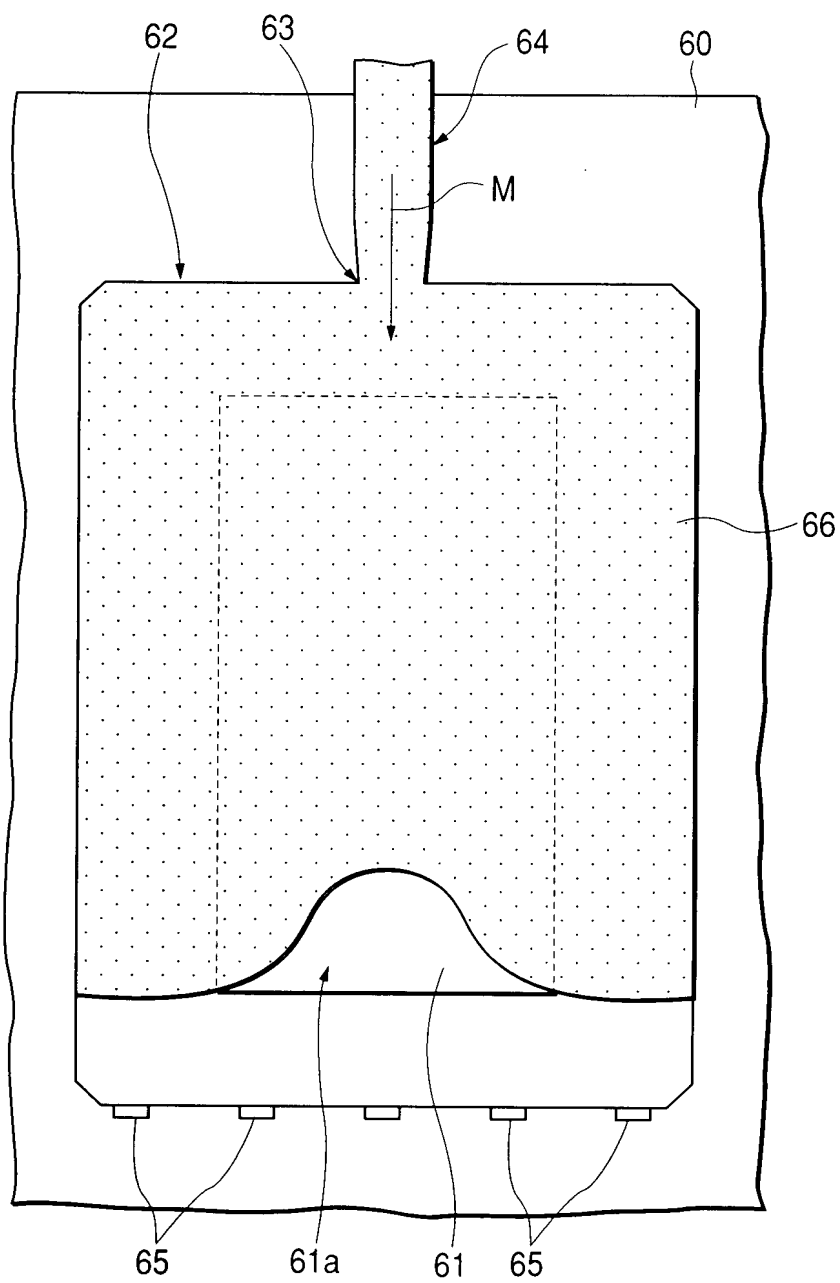


FIG. 34



20200924T600T

**FIG. 36**

